Refine Search

Search Results -

Term	Documents
(5 AND 16).PGPB,USPT.	0
(L16 AND L5).PGPB,USPT.	0

Database:
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Search History

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Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT; PLUR=YES; OP=OR			
L29	L16 and l5	0	L29
L28	L15 and l5	0	L28
L27	L14 and l5	0	L27
L26	L13 and l5	1	L26
L25	L11 and l5	4	L25
L24	L23 and l5	1	L24
L23	(713/310-340)[CCLS]	3630	L23
L22	l10 and l16	4	L22
L21	l10 and l15	6	L21
L20	l10 and l14	3	L20
L19	l10 and l13	6	L19

L18	l10 and l12	47	L18
L17	l10 and l11	47	L17
L16	(710/60)[CCLS]	343	L16
L15	(370/230)[CCLS]	1435	L15
L14	(709/233)[CCLS]	457	L14
L13	(712/225,227)[CCLS]	1178	L13
L12	(712/2-300)![CCLS]	12294	L12
L11	(712/2-300)[CCLS]	12294	L11
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L10	l6 and l7 and payload	1597	L10
L9	L8 and l7	4	L9
L8	l5 and l6	21	L8
L7	L6 near12 bus	29004	L7
L6	(low$3 or fast$3 or high$3 or slow$3) near6 (speed or rate or clock)	2213048	L6
L5	(deactivat$5 or disabl$5) near8 (cpu or alu or execution) near15 ("not" near4 execut$5 or free or moment$7)	31	L5
DB=USPT; PLUR=YES; OP=OR			
L4	L1 and payload	0	L4
L3	L2 and payload	0	L3
L2	5559986.pn.	1	L2
L1	5634131.pn.	1	L1

END OF SEARCH HISTORY

Results for "(((disabl*, deactiv*) <and> (cpu, alu) <and> (command*, instruction))<in>metad..."

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(((disabl*, deactiv*) <and> (cpu, alu) <and> (command*, instruction))<in>metadata Search

Check to search only within this results set

» Key

Display Format: Citation Citation & Abstract

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
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IEEE STD	IEEE Standard

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1. **Fetch Halting on critical load misses**
   Mehta, N.; Singer, B.; Bahar, R.I.; Leuchtenburg, M.; Weiss, R.;
   Computer Design: VLSI in Computers and Processors, 2004. ICCD 2004. Proceedings. IEEE Inter
   on
   11-13 Oct. 2004 Page(s):244 - 249
   Digital Object Identifier 10.1109/ICCD.2004.1347929
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2. **A low-power microcontroller with on-chip self-tuning digital clock-generator for variable-loa**
   Olivieri, M.; Trifiletti, A.; De Gloria, A.;
   Computer Design, 1999. (ICCD '99) International Conference on
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3. **Architectural and compiler support for energy reduction in the memory hierarchy of high pe microprocessors**
   Hajj, N.B.M.; Polyckronopoulos, C.; Stamoulist, G.;
   Low Power Electronics and Design, 1998. Proceedings. 1998 International Symposium on
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4. **Architectural and compiler techniques for energy reduction in high-performance microproce**
   Bellas, N.; Hajj, I.N.; Polychronopoulos, C.D.; Stamoulis, G.;
   Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
   Volume 8, Issue 3, June 2000 Page(s):317 - 326
   Digital Object Identifier 10.1109/92.845897
   AbstractPlus | References | Full Text: PDF(248 KB) IEEE JNL
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5. **Multi-level approaches to low power 16-bit ALU design**
   Beom Seon Ryu; Hyoung Sok Oh; Kie Hak Shim; Kie Young Lee; Tae Won Cho;
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   23-25 Aug. 1999 Page(s):158 - 161
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6. **A design of low power 16-b ALU**
Beom Seon Ryu; Jung Sok Yi; Kie Young Lee; Tae Won Cho;
TENCON 99. Proceedings of the IEEE Region 10 Conference
Volume 2, 15-17 Sept. 1999 Page(s):868 - 871 vol.2
Digital Object Identifier 10.1109/TENCON.1999.818556
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